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	Complete if Known	OIPE	
Application Number	09/963,735	1	_
Filing Date	09-27-2001	Nov	\vdash
First Named Inventor	Nobuo FUDANUKI	NOV 1 3 2002	†
Group Art Unit	2819	2 2	ተ
Examiner Name	Unassigned	(F)	_
Attorney Docket Number	016910-0476	RADEMARIA	_

U.S. PATENT DOCUMENTS							
Examiner Initials*		U.S. Patent Document			Date of Publication of	Pages, Columns, Lines,	
	Cite No. ¹	Number	Kind Code ² (if known)	Name of Patentee or Applicant of Cited Document	Cited Document MM-DD-YYYY	Where Relevant Passages or Relevant Figures Appear	
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W	A1	JP	1-100942		Semiconductor Integrated Circuit	04-19-1989		Х
he	A2	JP	61-253831		Standard Cell Semiconductor Apparatus	11-11-1986		×

		OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
w	A3	"A Versatile VLSI Design System for Combining Gate Array and Standard Cell Circuits on the Same Chip," Robert Homung, Martine Bonneau and Bernard Waymel, IEEE 1987 Custom Integrated Circuits Conference.	nif
			

Examiner Signature	00 N	Œ	Date Considered	7/1/03

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not ig conformance and not considered. Include copy of this form with next communication to applicant.

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